

DATA SHEET



BSR62 PNP Darlington transistor

Product specification
Supersedes data of 1999 Apr 26

2004 Nov 11

PNP Darlington transistor

BSR62

FEATURES

- High current (max. 1 A)
- Low voltage (max. 80 V)
- Integrated diode and resistor.

APPLICATIONS

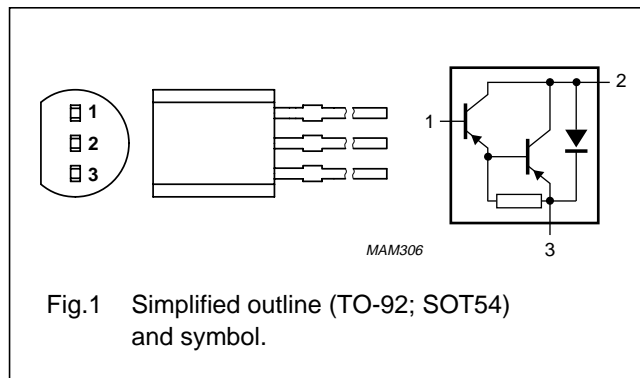
- Industrial applications such as:
 - Print hammer
 - Solenoid
 - Relay and lamp driving.

DESCRIPTION

PNP Darlington transistor in a TO-92; SOT54 plastic package. NPN complement: BSR52.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BSR62	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–90	V
V_{CES}	collector-emitter voltage	$V_{BE} = 0\text{ V}$	–	–80	V
V_{EBO}	emitter-base voltage	open collector	–	–5	V
I_C	collector current (DC)		–	–1	A
I_{CM}	peak collector current		–	–2	A
I_B	base current (DC)		–	–0.2	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	830	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	ambient temperature		–65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1	150	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

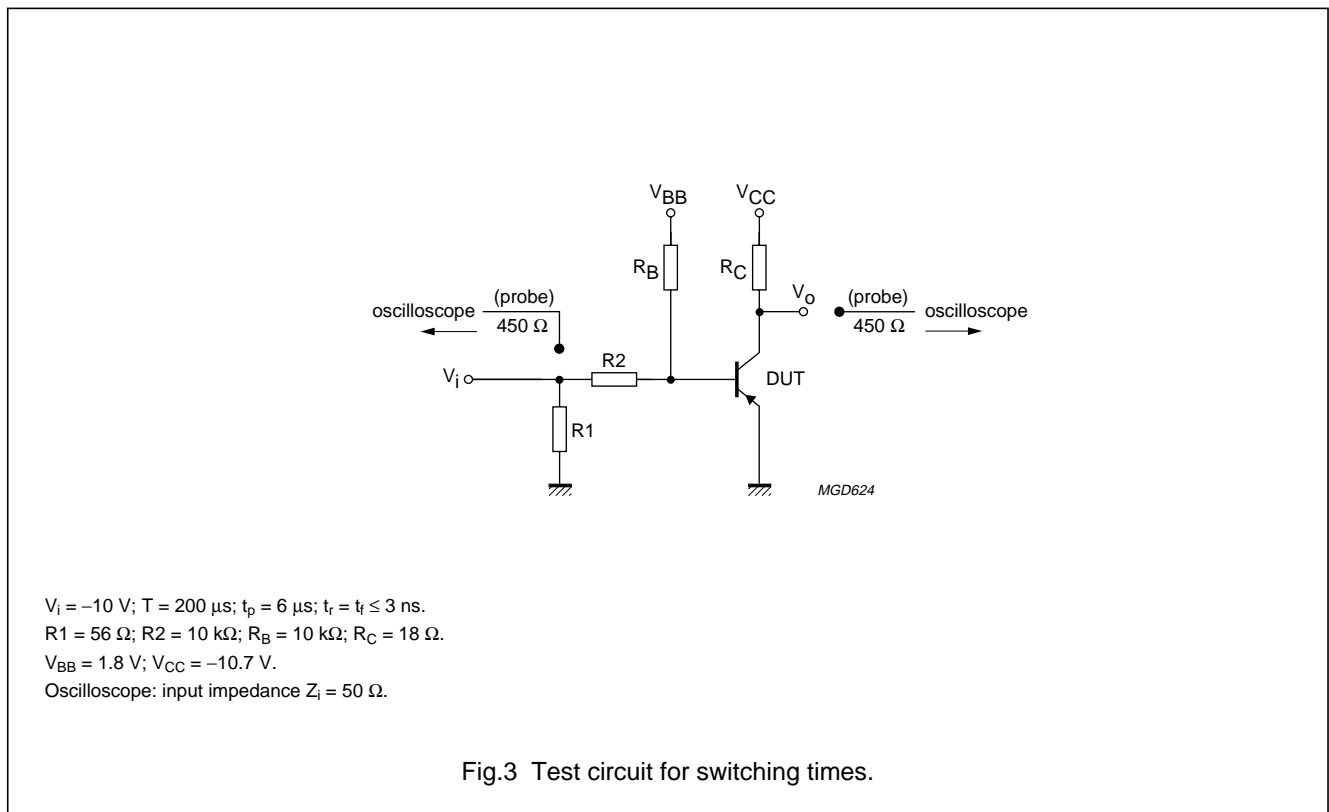
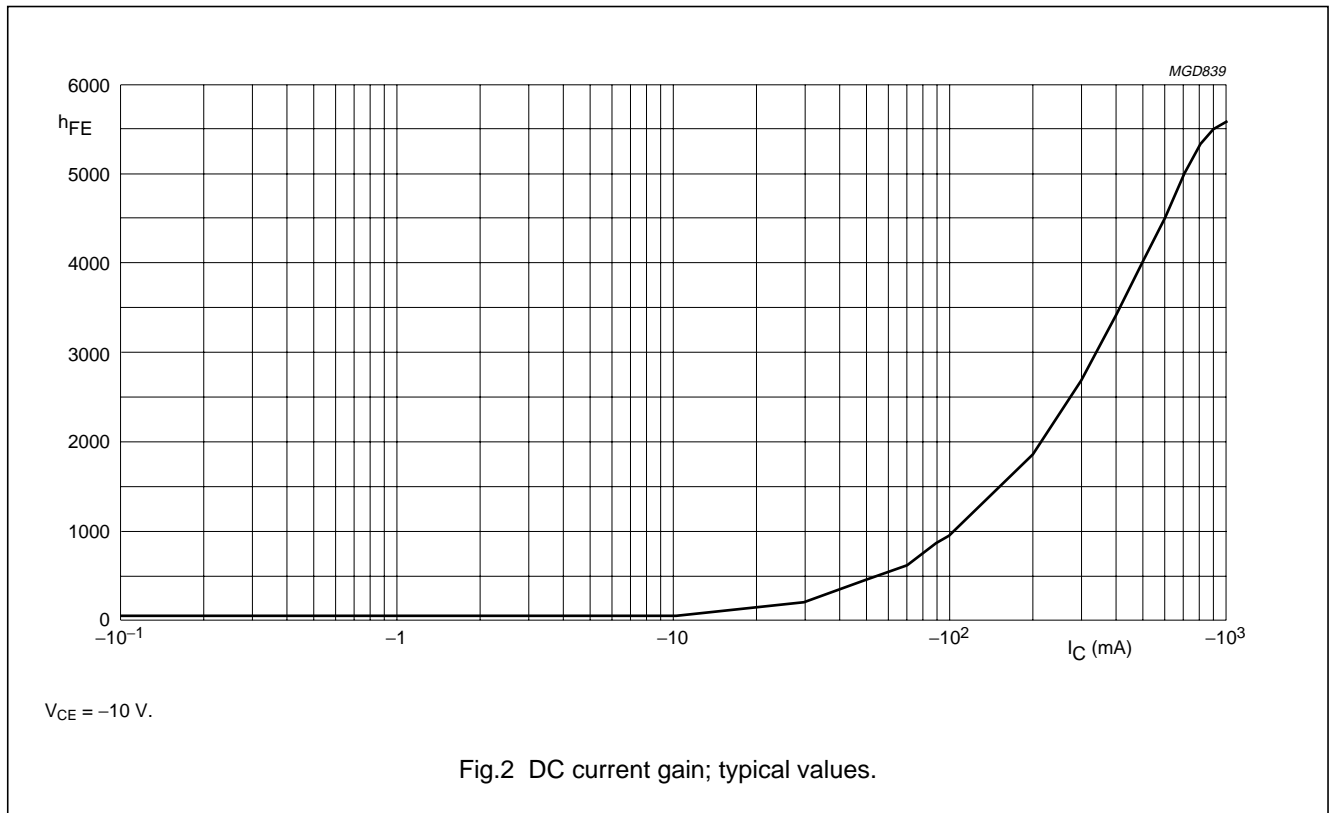
CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CES}	collector-emitter cut-off current	$V_{BE} = 0\text{ V}; V_{CE} = -80\text{ V}$	–	–	–50	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -4\text{ V}; I_C = 0\text{ A}$	–	–	–50	nA
h_{FE}	DC current gain	$V_{CE} = -10\text{ V}$; see Fig.2 $I_C = -150\text{ mA}$ $I_C = -500\text{ mA}$	1000 2000	– –	– –	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -0.5\text{ A}; I_B = -0.5\text{ mA}$	–	–	–1.4	V
		$I_C = -1\text{ A}; I_B = -4\text{ mA}$	–	–	–1.8	V
V_{BEsat}	base-emitter saturation voltage	$I_C = -0.5\text{ A}; I_B = -0.5\text{ mA}$	–	–	–2	V
		$I_C = -1\text{ A}; I_B = -4\text{ mA}$	–	–	–2.4	V
f_T	transition frequency	$V_{CE} = -5\text{ V}; I_C = -500\text{ mA};$ $f = 100\text{ MHz}$	–	200	–	MHz
Switching times (between 10% and 90% levels); see Fig.3						
t_{on}	turn-on time	$I_{Con} = -500\text{ mA}; I_{Bon} = -0.5\text{ mA};$	–	–	0.5	μs
t_{off}	turn-off time	$I_{Boff} = 0.5\text{ mA}$	–	–	0.7	μs

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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT54		TO-92	SC-43A		-97-02-28 04-06-28

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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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